Sub A1

ABSTRACT

A programmable pipeline depth controller is provided to control the number of instructions that begins execution within an instruction pipeline of an instruction processor within a predetermined period of time. The pipeline depth controller of the present invention includes a logic sequencer responsive to a programmable count value. Upon being enabled, the logic sequencer generates a pipeline control signal to selectively delay the entry of some instructions into the instruction pipeline. As a result, the number of instructions that begins execution within the instruction pipeline during the predetermined period of time following the enabling of the logic sequencer is equal to the count value. The flow of instructions through the instruction pipeline may be adjusted by re-programming the count value. Various modes of operation are provided for the pipeline depth controller. According to one mode, the pipeline depth controller is enabled to repeatedly generate the pipeline control signal in response to the selected count value. As a result, the number of instructions entering the pipeline during any period of time that is equal to the predetermined period of time is dictated by the count value. A second mode of operation is provided to enable the pipeline control signal to be generated in response to the entry of any of one or more selected instructions into the instruction pipeline. When one of the selected instructions enters the pipeline, the pipeline depth controller is enabled and is provided with a respective count value. During the predetermined period of time after the pipeline depth controller is enabled, the logic sequencer limits the number of instructions that enters the instruction pipeline to that number dictated by the count value. After the predetermined period of time elapses, the pipeline depth controller is disabled and the instruction pipeline continues execution in default mode. According to yet another mode of operation, the pipeline depth controller is enabled when any of one or more selected combinations of instructions enters the pipeline. Each defined instruction combination may be associated with a respective count value. In this instance, the logic sequencer asserts control in a manner similar to that described above with respect to the entry of a single selected instruction into the pipeline. Still another mode allows the pipeline depth controller to be conditioned such that pipeline control is asserted only when a particular instruction combination enters the instruction pipeline while a particular system condition, such as a predetermined error, is occurring.